Digital Electronics and VHDL

Practical 7 - SEQUENTIAL MACHINES

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## **IMPORTANT UPDATES – READ THIS BEFORE YOU START**

With each year, there may be some minor updates to the tools. These are documented here. Please read this section before you begin.

### Target FPGA

The Cyclone II device sometimes featured in the videos is no longer supported in Quartus. We are currently using a **Cyclone® IV EP4CE22F17C6**

### Quartus II and the Vector Waveform Editor

Since version 13, Altera reinstated the vector waveform editor directly into Quartus II. This has not changed since v13. Some of the videos may make reference to an external tool. The tool is fundamentally the same, but now you can add a “vector waveform file” directly into your project from Quartus (File->New->… VWF)

To see how this has changed, please refer to the video “Using Quartus 13+ with VWF HD.mp4”

### Quartus User Interface

With each version that is released, the user interface can sometimes change in appearance. With version 16, the user interface has been noticeably re-skinned. However, the same basic functionality is still available from the menus as tool bar (the icons are now more colourful). To find the new icon, if necessary you can hover your mouse over the toolbar buttons, and you will see a text prompt. Given we only use a small subset of the buttons, it was not deemed necessary on this occasion to re-record the tutorial videos.

# Introduction

We will now begin to look at some sequential applications in VHDL. In particular, we will look at how we begin to build finite state machines (for digital control) and serial interfaces. Topics will include:

* Shift Registers
* Finite State Machines
* Multiple process blocks

# 01 - SHIFT REGISTERS

The four basic categories of shift register are shown below (control signals not shown). There a number of different variants and applications of shift registers, and one important example is serial interfacing. Before we look at serial interfaces, let's first look at two important categories of shift register which make up the basis of many serial interface devices: parallel-to-serial and serial-to-parallel.

|  |  |  |
| --- | --- | --- |
|  | Serial In | Parallel In |
| Serial  Out |  |  |
| Parallel  Out |  |  |

## Parallel to Serial Conversion

You may be familiar with the circuit below. This is a 4-bit **synchronous** parallel-to-serial converter.



|  |
| --- |
| Synchronous parallel to serial converter |
| Why is this considered to be **synchronous** |
|  |
| What is the function of the input? |
|  |
| If we wanted to scale this circuit up to 32 bits, are there any problems with scalability? |
|  |

*Discuss your solutions with the tutor.....*

Let's now look at how we might build this in VHDL.

**entity** uop\_shiftreg\_p2s **is**

**generic** ( N : **positive** := 8);

**port**

(

--Inputs

CLK : **in** std\_logic;

DATA\_IN : **in** std\_logic\_vector( (N-1) **downto** 0 );

LOAD : **in** std\_logic;

RESET : **in** std\_logic;

--Outputs

DATA\_OUT : **out** std\_logic

);

**end** **entity**;

**architecture** p2s **of** uop\_shiftreg\_p2s **is**

**begin**

**process** (CLK) **is**

**variable** idx : integer := 0;

**variable** Nreg : std\_logic\_vector( (N-1) **downto** 0 );

**begin**

**if** (RESET='0') **then**

idx := 0;

Nreg := (others => '0');

**elsif** (CLK'event and CLK = '1') **then**

**if** (LOAD = '1') **then**

Nreg := DATA\_IN;

idx := 0;

DATA\_OUT <= Nreg(idx);

**elsif** (idx < (N-1)) **then**

idx := idx + 1;

DATA\_OUT <= Nreg(idx) **after** 2 ps;

**end if;**

**end if;**

**end process;**

**end p2s;**

|  |
| --- |
| Synchronous parallel to serial converter |
| Open Task 01-01 |
| Build and simulate using the testbench uop\_shiftreg\_p2s.vht (remember to compile it first!) |
| Read through the VHDL (and the comments) |
| **Question:**  There is an implicit latch in this architecture. Can you identify where it is?  What is causing the latching behavior?  Is the data sent most or least significant bit first?  When the parallel data is loaded into the internal register, how many clock cycles does it take for the first bit appear on the output?  Note the timing of the LOAD input in relation to the clock edge. Why is the LOAD signal timed the way it is? |

You might have noticed the following line:

DATA\_OUT <= Nreg(idx) **after** 2 ps;

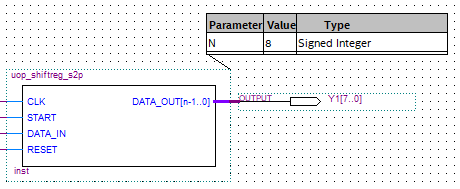
This is to give the simulation has *some* propagation delay in the output. This helps to model a real system more realistically. If we were to perform “gate level simulation”, these delays would be inserted in multiple places by Quartus.

Creating a shift register such as this is not overly complex, but a shift register alone is not generally sufficient when designing a serial interface. Generating the correct timing signals requires more thought and careful control!

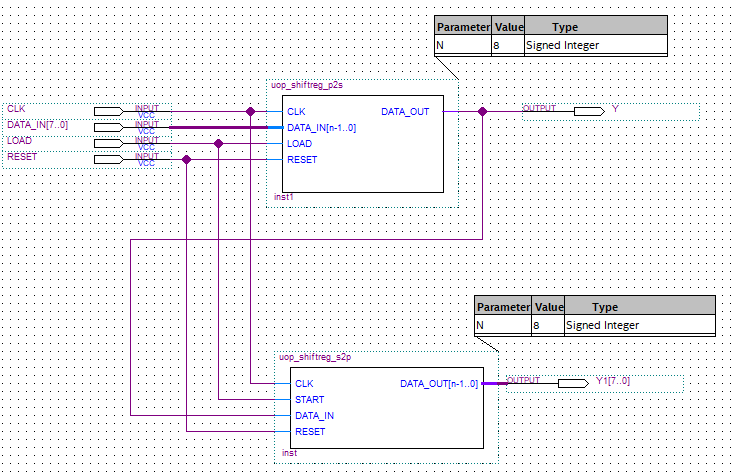
Consider designing another circuit (e.g., serial to parallel) that receives the serial bits and reconstructs them into a (latched) parallel word. Whatever circuit is receiving the serial stream, whether synchronous or asynchronous, it will need to know **when to start reading the bits and when to stop**. Some form of "**protocol**" is often required to ensure timing is perform correctly and "kept in sync". This is usually orchestrated by a state-machine.

## Serial to Parallel shift register

Let's now look at the converse operation, converting a series of serial bits to a parallel word. First, let's look at the entity.



For inputs, there is a clock input (CLK), a serial data in (DATA\_IN), a control line (START) and a reset (RESET). For outputs, there is a parallel N-bit wide output DATA\_OUT. Now let us look at the context in which it is used:



Note two devices use a shared clock and reset. Furthermore, the LOAD signal and the START signal are connected[[1]](#footnote-1). There are some subtle timing issues with designs like this, but this will be discussed later. For now, let us look at the serial to parallel converter.

The VHDL is given below. Note again the use of generics to make this entity more general purpose.

**entity** uop\_shiftreg\_s2p **is**

**generic** ( N : **positive** := 8);

**port**

(

--Inputs

CLK : **in** std\_logic;

START : **in** std\_logic;

DATA\_IN : **in** std\_logic;

RESET : **in** std\_logic;

--Outputs

DATA\_OUT : **out** std\_logic\_vector( (N-1) **downto** 0 )

);

**end entity;**

The architecture for this entity is given below:

**architecture** s2p **of** uop\_shiftreg\_s2p **is**

**type** state\_type **is** (WAITING, SHIFTING);

-- Register to hold the current state

**signal** state : state\_type;

**begin**

**process** (CLK,RESET) **is**

**variable** Nreg : std\_logic\_vector( (N-1) **downto** 0 );

**variable** idx : integer := 0;

**begin**

**if** (RESET = '0') **then**

Nreg := (**others**=>'0');

state <= WAITING;

DATA\_OUT <= (**others**=>'0');

**else**

**if** rising\_edge(CLK) then

**case** state **is**

**when** WAITING=>

**if** START = '1' **then**

idx := 0;

state <= SHIFTING;

**end if;**

**when** SHIFTING=>

Nreg(idx) := DATA\_IN;

idx := idx + 1;

**if** (idx = N) **then**

state <= WAITING;

DATA\_OUT <=Nreg;

**end if;**

**end case;**

**end if;**

**end if;**

**end process;**

**end s2p;**

This is the receiver which converts serial data to parallel. Remember – the transmitter (parallel to serial) is writing its data on the RISING EDGE of the clock. Keep this is mind!

|  |
| --- |
| Synchronous serial to parallel converter |
| **Question -** Is this device output triggered on the rising or falling edge of the clock? |
| Open task 01-02 |
| Build then launch ModelSim. Now simulate using the testbench uop\_shiftreg\_s2p.vht (remember to compile it first) |
| Examine the testbench. Check the output agrees with expectation |
| Next, we can see if the whole system is working. The top level schematic has already been converted to VHDL for you (top\_level.vhd). Compile top top\_level.vhd and then the test benchg top\_level.vht |
| Simulate top\_level.vht to see a full parallel to serial, and then it converted back to parallel again. You should see the input data appearing in the output, albeit delayed. This demonstrates a successful transmission of data over a serial wire. |
| Read through the test bench to see how it works |
| **Questions**  The parallel to serial converter writes the serial data *on the rising edge of the clock*.   * Once START goes HIGH, how many clock cycles does the serial-to-parallel device wait until reading the input and why is this necessary? * If the output device is writing serial data on the rising edge of the clock, and the input is also reading on the same rising clock edge, how is it that we not invalidating the setup and hold times?  We are assuming the internal logic to have a finite setup time and 0ps hold time.   *hint:* this work for the same reason you can cascade D-Type flipflops. *This is not an easy question to answer.* Also remember that we purposely modeled some propagation delay on the output of the transmitter (parallel to serial). |

**Comments:**

Sequential logic is much more complex than combinational. One of the biggest challenges is avoiding timing errors, and these can be hard to spot. In the previous example, a few issues were highlighted.

Pure functional simulations can be misleading. In real circuits, propagation delay is unavoidable, and in some cases, is a requirement for circuits to work as expected. A good example of this is with shift registers.

Consider what happens **on each rising edge of the clock**:

* For the transmitter:
  + This is when the serial data is written to the serial line.
  + There is always some propagation delay, so the signal changes Tpd **after** the clock edge.
* For the receiver:
  + Data is read on the clock edge.
  + If the signal on the input is stable Tsetup before the clock edge, there is no metastability.
  + If the signal on the input is stable Thold after the clock edge, there is no metastability.
    - For this to work, we therefore require Thold < Tpd
    - For D-Type flip-flops, Thold is zero so this is not an issue.
  + In effect, *the receiver reads the (stable) output from the previous clock cycle*.

The behavioral VHDL style rather masks this as we do not see the flip-flops.

# 02 - Finite State Machines

One of the most common general sequential designs is a finite state machine. In this example, we are going to consider a "Moore Machine" - one where the outputs are purely a function of the **state**.

Recall that the **state** is simply a number which records where we are in some sequence. For each state, on every clock edge, we define the outputs and the next state.



In VHDL, a state machine can easily be implemented. An example is given in task 02-01

## TASK 02-01 Tracking an Input Sequence

In this task, you are going to use a finite state machine to detect a pre-defined sequence of input bits. Finite state machines fit well with VHDL and are almost self-documenting.

|  |
| --- |
| Finite State Machine - Detecting an input sequence |
| Open Task 02-01 |
| Examine the top level schematic and the entity "moore\_state\_machine.vhdl" |
| Can you draw the state diagram for this VHDL code? Show the tutor. |
| Build and run the simulation. DATA\_IN is the (simulated) input from a push switch |
| Does the output agree with what you expect? |

This is such a common pattern that there is a template in Quartus to help you get started.

Did you notice that there were **two process blocks** in this design? Each process block is a piece of parallel hardware (within each process block, we describe the expected behavior sequentially of course).

Discuss with the tutor if you do not understand this.

## TASK02-02 - Generating a Sequence

Sometimes you can use a state machine to generate one or more sequences with each clock edge.

|  |
| --- |
| Finite State Machine - Sequence Generator |
|  |
| Copy Task 02-01 and rename to Task 02-02 |
| Create a new VHDL file |
| Right Click and click on "Insert Template" |
| Select VHDL->Full Designs->State Machines->Four-State-Moore-State-Machine |
| Click Insert then Close |
| Save the VHDL file as uop\_pattern\_gen.vhdl |
| Modify the VHDL to implement the state machine described below |
| Simulate and test |
| (a solution is also provided) |

Figure 1 is a finite state machine design for a pattern generator. While the RESET is held low, the output Y is held LOW. When RESET=1, a 4-bit output sequence is generated. The input "Pattern" selects the sequence pattern to generate. Note that RESET is an input and it synchronous.

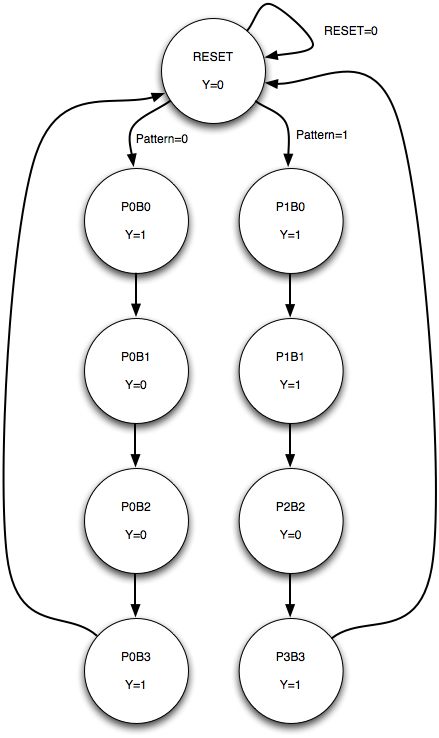


Figure . Finite State Diagram. Two synchronous inputs RESET and Pattern; One output bit Y

# Appendix A – entities and architectures

## Entity

**entity** entity-name **is**

**port** (signal-names : mode signal-type [ := initial value ];

**port** (signal-names : mode signal-type [ := initial value ];

**port** (signal-names : mode signal-type [ := initial value ]

**end** entity-name;

**NOTE** – no semi-colon here!

|  |  |
| --- | --- |
| **Item** | **DESCRIPTION** |
| Entity-name | A name you choose, that matches the filename |
| Signal-names | A comma separated list of one or more input or output signals |
| Mode | This can be:  in – input  out – output  buffer – an output that can be read from within the architecture  inout – input or output, normally associated with tri-state outputs on PLD’s |
| Signal-type | The signal type. See Appendix B for pre-defined types. You can also create your own. |

## Architecture

**architecture** architecture-name if entity-name **is**

-- local variables, types etc…

type declarations

signal declarations

constant declarations

function definitions

procedure definitions

component declarations

**begin**

concurrent statement 1

concurrent statement 2

**end** architecture-name;

# APPENDIX B – PREDEFINED TYPES AND OPERATORS

## VHDL PREDEFINED TypeS

|  |  |
| --- | --- |
| **TYPE** | **DESCRIPTION** |
| bit | Single bit that takes values '0', '1' |
| bit\_vector | Vector (array) of bits |
| boolean | *true* or *false* |
| character | ISO 8-bit character |
| integer | Whole number between |
| real | Fractional numbers |
| severity\_level |  |
| string |  |
| time |  |

## VHDL Comparison operators

|  |  |
| --- | --- |
| **OPERATOR** | **DESCRIPTION** |
| = | Equals |
| /= | Not equals |
| > | Greater than |
| < | Less than |
| >= | Greater than or equal |
| <= | Less than or equal |

## VHDL INTEGER Operators

|  |  |
| --- | --- |
| **OPERATOR** | **DESCRIPTION** |
| + | Addition |
| - | Subtraction |
| \* | Multiplication |
| / | Division |
| Mod | Modulo division |
| Rem | Modulo remainder |
| Abs | Absolute value |
| \*\* | Exponentiation |

## VHDL Shifting Functions

|  |  |
| --- | --- |
| **OPERATOR** | **DESCRIPTION** |
| sll | Shift left logical |
| srl | Shift right logical |
| sla | Shift left arithmetic (preserve sign bit) |
| sra | Shift right arithmetic (preserve and copy sign bit) |
| rol | Rotate left |
| ror | Rotate right |

## VHDL BINARY OPERATORS

|  |  |
| --- | --- |
| **OPERATOR** | **DESCRIPTION** |
| and | AND |
| or | OR |
| nand | NAND |
| nor | NOR |
| xor | Exclusive OR |
| xnor | Exclusive NOR |
| not | Compliment (Inverter) |

# Appendix C - Concurrent statements

## When-Else

*signal-name* <= *expression* **when** *boolean-expression* **else**

*expression* **when** *boolean-expression* **else**

...

...

*expression* **when** *boolean-expression* **else**

*expression*;

## SELECT

**with** *expression* **select**

*signal-name* <= *signal-value* **when** *choices*,

*signal-value* **when** *choices*,

...

..

*signal-value* **when** *choices,*

*signal-value* **when****others**;

# Appendix D - TYPE and subtype DEFINTIONS

**type** *type-name* **is** (*value list*);

**subtype** *subtype-name* **is** *type-name* **range** *start* **to** *end*;

**subtype** *subtype-name* **is** *type-name* **range** *start* **downto** *end*;

**constant** *constant-name*: *type-name* := *value*;

# Appendix E - Arrays

**type** *type-name* **is** **array** (*start* **to** *end*) **of** *element-type*;

**type** *type-name* **is** **array** (*start* **downto** *end*) **of** *element-type*;

**type** type-name **is** **array** (*range-type*) **of** *element-type*;

**type** type-name **is** **array** (*range-type* **range** *start* **to** *end*) **of** *element-type*;

**type** type-name **is** **array** (*range-type* **range** *start* **downto** *end*) **of** *element-type*;

**type** *type\_name* **is array** (*type* **range <>) of** *element\_type*; -- unconstrained array

# APENDIX F - IEEE STD\_ULOGIC and STD\_LOGIC

**type** STD\_ULOGIC **is** ( 'U', -- uninitialized

'X', -- forcing unknown

'0', -- forcing 0

'1', -- forcing 1

'Z', -- High Impedance

'W', -- Weak unknown

'L', -- Weak 0

'H', -- Weak 1

'-', -- Don't care

);

**subtype** STD\_LOGIC **is resolved** STD\_ULOGIC;

-- and the vectors

**type** STD\_ULOGIC\_VECTOR **is array** (natural **range** <>) **of** STD\_ULOGIC;

**type** STD\_LOGIC\_VECTOR **is array** (natural **range** <>) **of** STD\_LOGIC;

# Appendix G - Structural statements

## component Declaration

**component** *component-name*

**port** ( *signal-names* : *mode* *signal-type*;

*signal-names* : *mode* *signal-type*;

...

*signal-names* : *mode* *signal-type )*;

**end component**;

## Instantiation

*label: component-name* **port map** (*signal1, signal2, ..., signaln*);

*label: component-name* **port map** (*port1=>signal1, port2=>signal2, ..., portn=>signaln*);

## Generate

*label*: **for** *identifier* **in** *range* **generate**

*concurrent-statement*

**end generate;**

## Generic Declarations

**generic** ( *constant-names* : *constant-type*;

*constant-names* : *constant-type*;

...

*constant-names* : *constant-type*);

# Appendix H - Behavioural Statements

## process statement

**process** (*signal-name, signal-name, ..., signal-name*)

*type declarations*

*variable declarations*

*constant declarations*

*function definitions*

*procedure definitions*

**begin**

*sequential statement*

*sequential statement*

*...*

*sequential statement*

**end process;**

## if statement

**if** *boolean-expression* **then** *sequential-statements*

end if;

## If-ELSe

**if** *boolean-expression* **then** *sequential-statements*

**else** *sequential-statements*

**end if;**

## if-elsif

**if** *boolean-expression* **then** *sequential-statements*

**elsif** *boolean-expression* **then** *sequential-statements*

**elsif** *boolean-expression* **then** *sequential-statements*

...

**elsif** *boolean-expression* **then** *sequential-statements*

**end if;**

## if-elsif-ELSE

**if** *boolean-expression* **then** *sequential-statements*

**elsif** *boolean-expression* **then** *sequential-statements*

**elsif** *boolean-expression* **then** *sequential-statements*

...

**elsif** *boolean-expression* **then** *sequential-statements*

**else** *sequential-statements*

**end if;**

## CASE

**case** expression **is**

**when** choices => sequential-statements

**when** choices => sequential-statements

...

**when** choices => sequential-statements

**end case;**

## LOOP

**loop**

*sequential-statement*

*sequential-statement*

*...*

*sequential-statement*

*[****next*** *[label] [****when*** *condition];*

*[****exit*** *[label] [****when*** *condition];*

**end loop**;

## FOR LOOP

**for** identifier **in** range **loop**

*sequential-statement*

*sequential-statement*

...

*sequential-statement*

*[****next*** *[label] [****when*** *condition];*

*[****exit*** *[label] [****when*** *condition];*

**end loop**;

## while loop

**while** boolean-expression **loop**

*sequential-statement*

*sequential-statement*

...

*sequential-statement*

*[****next*** *[label] [****when*** *condition];*

*[****exit*** *[label] [****when*** *condition];*

**end loop**;

## NEXT and EXIT

The **next** statement skips to the next iteration of the loop.

The **exit** statement skips the reset of the statements in the loop body and breaks out of the loop.

# Appendix I - STANDARD ATTRIBUTES

*(from http://www.cs.umbc.edu/portal/help/VHDL/attribute.html, accessed 4/11/2010)*

**T** represents any type

**A** represents any array or constrained array type

**S** represents any signal

**E** represents a named entity

## Type Attributes

**T'BASE** *is the base type of the type T*

**T'LEFT** *is the leftmost value of type T (Largest if using downto)*

**T'RIGHT** *is the rightmost value of type T. (Smallest if using downto)*

**T'HIGH** *is the highest value of type T*

**T'LOW** *is the lowest value of type T*

**T'ASCENDING** *is Boolean true if range and T defined with 'to'*.

**T'IMAGE(X)**  *is a string representation of X that is of type T*

**T'VALUE(X)**  *is a value of type T converted from the string X*

**T'POS(X)** *is the integer position of X in the discrete type T*

**T'VAL(X)**  *is the value of discrete type T at integer position X*

**T'SUCC(X)** *is the value of discrete type T that is the successor of X*

**T'PRED(X)** *is the value of discrete type T that is the predecessor of X*

**T'LEFTOF(X)** *is the value of discrete type T that is left of X*

**T'RIGHTOF(X)** *is the value of discrete type T that is right of X*

## Array Attributes

**A'LEFT** *is the leftmost subscript of array A or constrained array type*

**A'LEFT(N)** *is the leftmost subscript of dimension N of array A*

**A'RIGHT** *is the rightmost subscript of array A or constrained array type*

**A'RIGHT(N)** *is the rightmost subscript of dimension N of array A*

**A'HIGH** *is the highest subscript of array A or constrained array type*

**A'HIGH(N)** *is the highest subscript of dimension N of array A*

**A'LOW**  *is the lowest subscript of array A or constrained array type*

**A'LOW(N)** *is the lowest subscript of dimension N of array A*

**A'RANGE** *is the range A'LEFT to A'RIGHT or A'LEFT downto A'RIGHT*

**A'RANGE(N)** *is the range of dimension N of A*

**A'REVERSE\_RANGE** *is the range of A with to and downto reversed*

**A'REVERSE\_RANGE(N)** *is the REVERSE\_RANGE of dimension N of array A*

**A'LENGTH** *is the integer value of the number of elements in array A*

**A'LENGTH(N)** *is the number of elements of dimension N of array A*

**A'ASCENDING** *is boolean true if range of A defined with to*

**A'ASCENDING(N)** *is boolean true if dimension N of array A defined with to*

## SIGNAL ATTRIBUTES

**S'DELAYED(t)** *is the signal value of S at time now - t*

**S'STABLE** *is true if no event is occurring on signal S*

**S'STABLE(t)** *is true if no event has occurred on signal S for t units of time*

**S'QUIET** *is true if signal S is quiet (no event this simulation cycle)*

**S'QUIET(t)** *is true if signal S has been quiet for t units of time*

**S'TRANSACTION** *is a bit signal, the inverse of previous value each cycle S is active*

**S'EVENT** *is true if signal S has had an event this simulation cycle*

**S'ACTIVE** *is true if signal S is active during current simulation cycle*

**S'LAST\_EVENT** is the time since the last event on signal S

**S'LAST\_ACTIVE** *is the time since signal S was last active*

**S'LAST\_VALUE** *is the previous value of signal S*

**S'DRIVING** *is false only if the current driver of S is a null transaction*

**S'DRIVING\_VALUE** *is the current driving value of signal S*

**E'SIMPLE\_NAME** *is a string containing the name of entity E*

**E'INSTANCE\_NAME** *is a string containing the design hierarchy including E*

**E'PATH\_NAME** *is a string containing the design hierarchy of E to design root*

1. Real world serial interfaces typically use a different mechanism to coordinate when to start reading and writing [↑](#footnote-ref-1)